NetChip:
A Design Flow for Networks on Chips

Stergios Stergiou

Stanford University, CA, USA

Outline

- Motivation
- xpipes Lite Library Architecture
- NetChip Design Flow
- Experimental Results

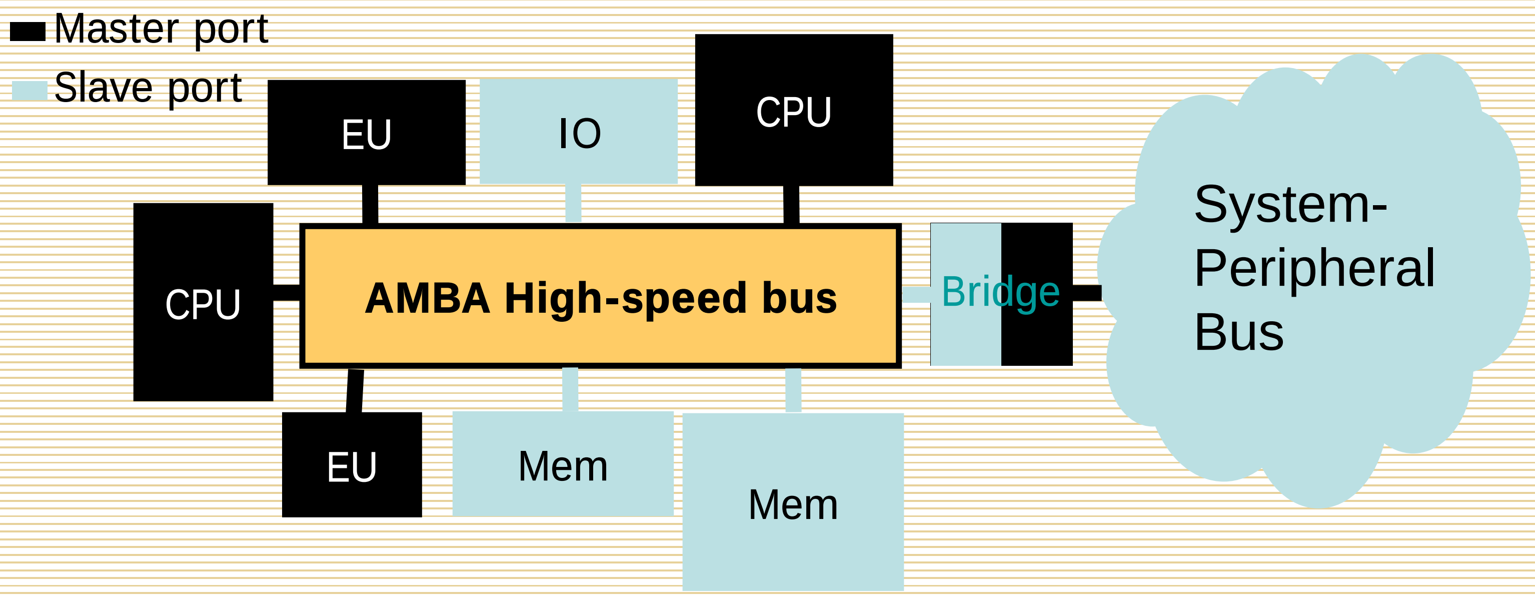
Motivation

- Design Complexity:
  - From 10 to 100+ Cores!
- Performance:
  - Requirements Go Up!
  - Power Budget Remains Fixed
- Scalability:
  - Current Architectures Cannot Keep Up!

Bus Architectures

- Sonics MicroNetwork
  - Highly Parameterizable, TDMA-based Bus
- STBus / AMBA
  - High Performance, Support Instantiation of Various Topologies

Example: *AMBA*

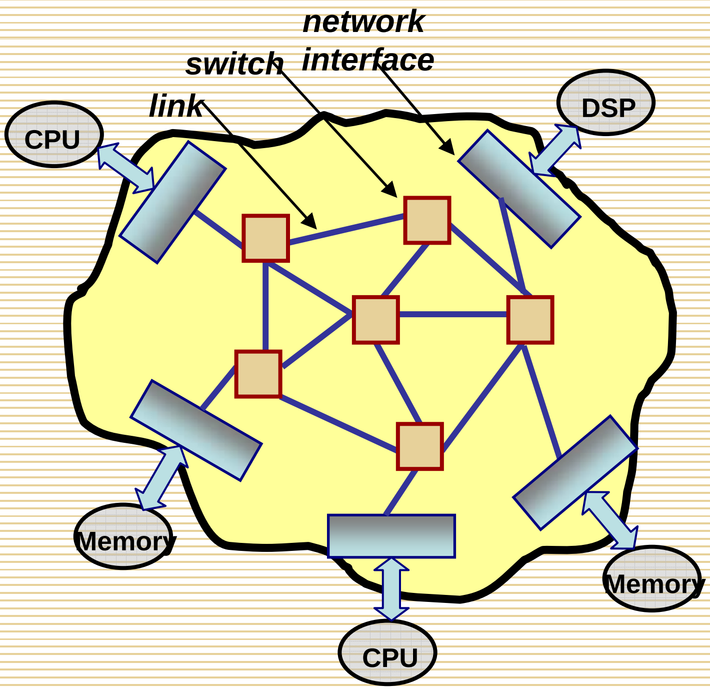


Bus Architectures

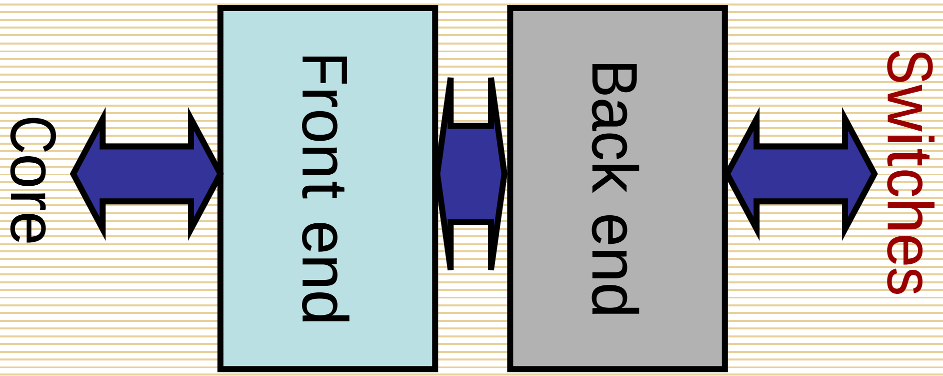
- Protocol
  - Lacks parallelism
  - *Traditionally:*
    - in order completion
    - no multiple outstanding transactions
- High arbitration overhead
- Bus architecture exposed
  - Hinders IP integration
- Topology
  - Scalability limitation of shared bus solution

Networks on Chips

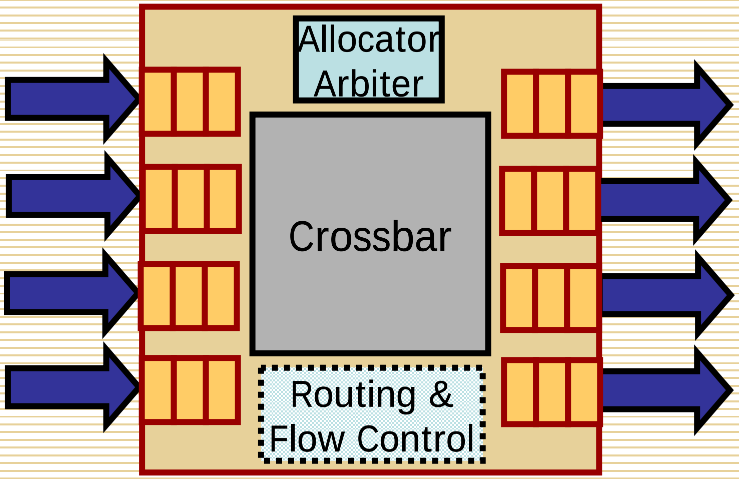
Network On Chip Topology



Network Interface



Switch Fabric



Networks on Chips

Previous Work

- NoC Architectures
  - SPIN, *DATE'00*
  - Dally & Towles, *DAC'01*
  - Aethereal, *DATE'03*
  - xpipes, *ICCD'03*
- Design Tools
  - Power Analysis: T. Ye et al, *DAC'02*
  - xpipes Compiler: A. Jalabert et al, *DATE'04*
- Industry
  - Arteris, STmicroelectronics

Xpipes Lite: Redesign

Xpipes Lite

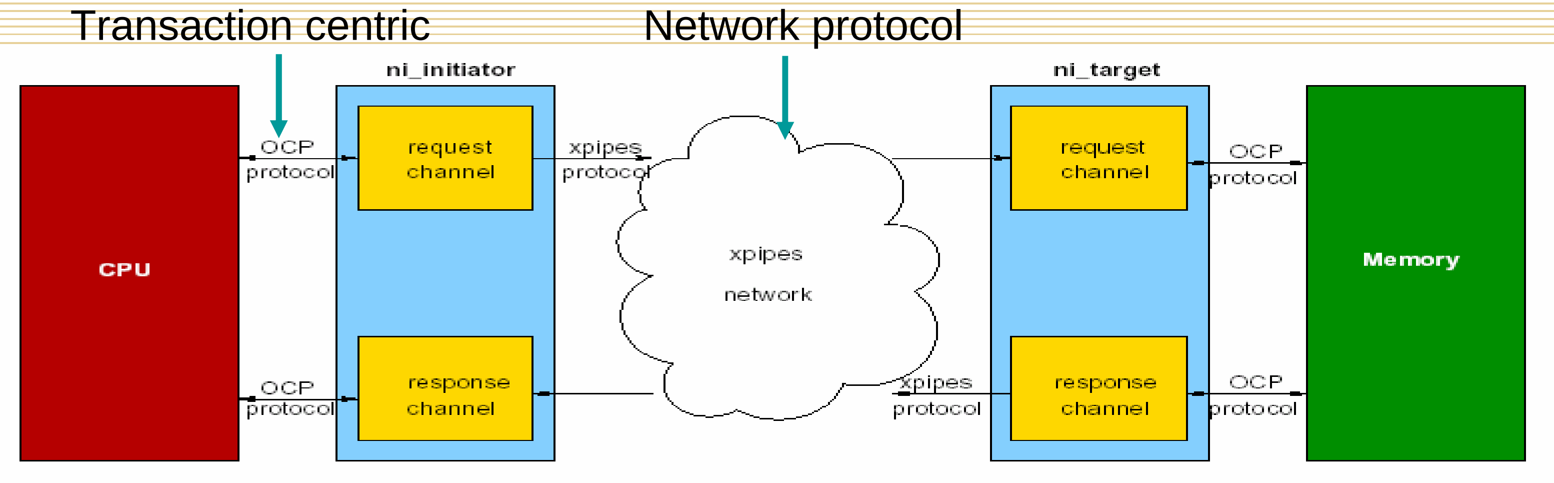
- Second xpipes Design Library Version
- *Complete* Redesign!
- Goals:
  - High Performance
  - Automated Synthesis
- Comparison With Original xpipes Library
  - Lower Latency (7 to 2 stage switches)
  - Fully Synthesizable!

Xpipes Lite: Network Interface

OCP

- End-to-end communication protocol
- Independent request/response
- Can be tailored to core features
- Support for sideband signals
  - interrupts
- Efficient burst handling
- Supports threading extensions

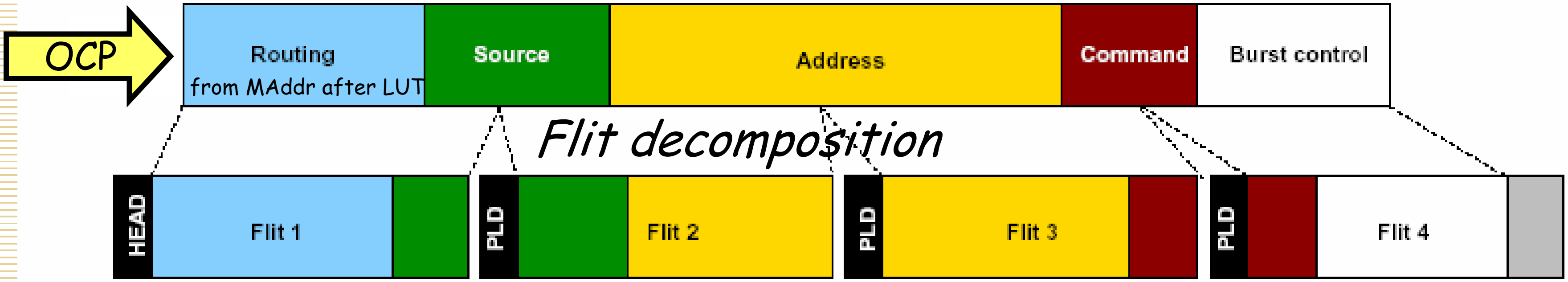
Network Interface



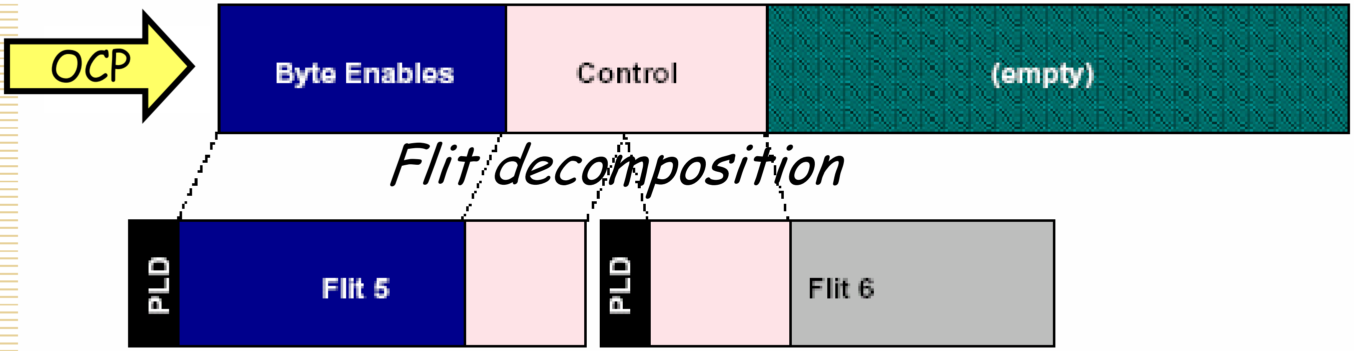
Xpipes Lite: Packetization

Packetization

Header register (about 50 bits): one for every transaction



Payload register: one for every burst beat

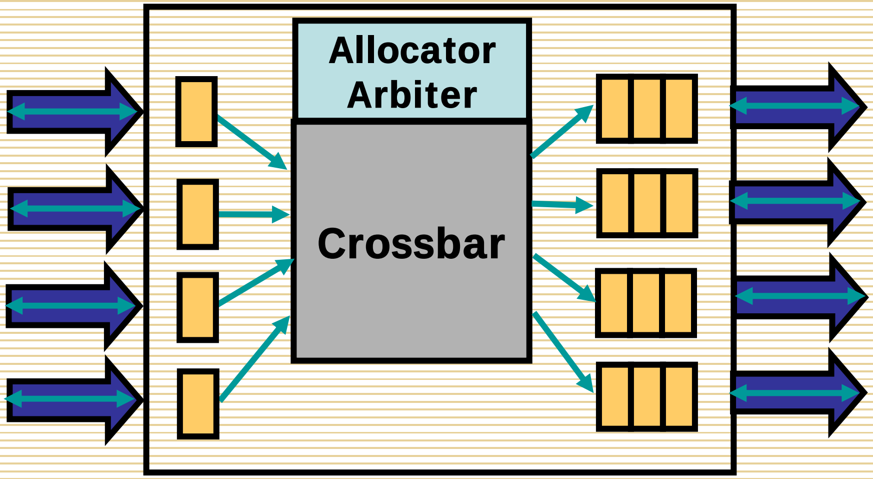


First beat of
a burst read

Xpipes Lite: Switch

- Output Queued
  - Buffering for Performance
  - ACK/nACK Flow & Error Control
- Support for Asymmetric Topologies
- Designed for Pipelined, Unreliable Links

Switch

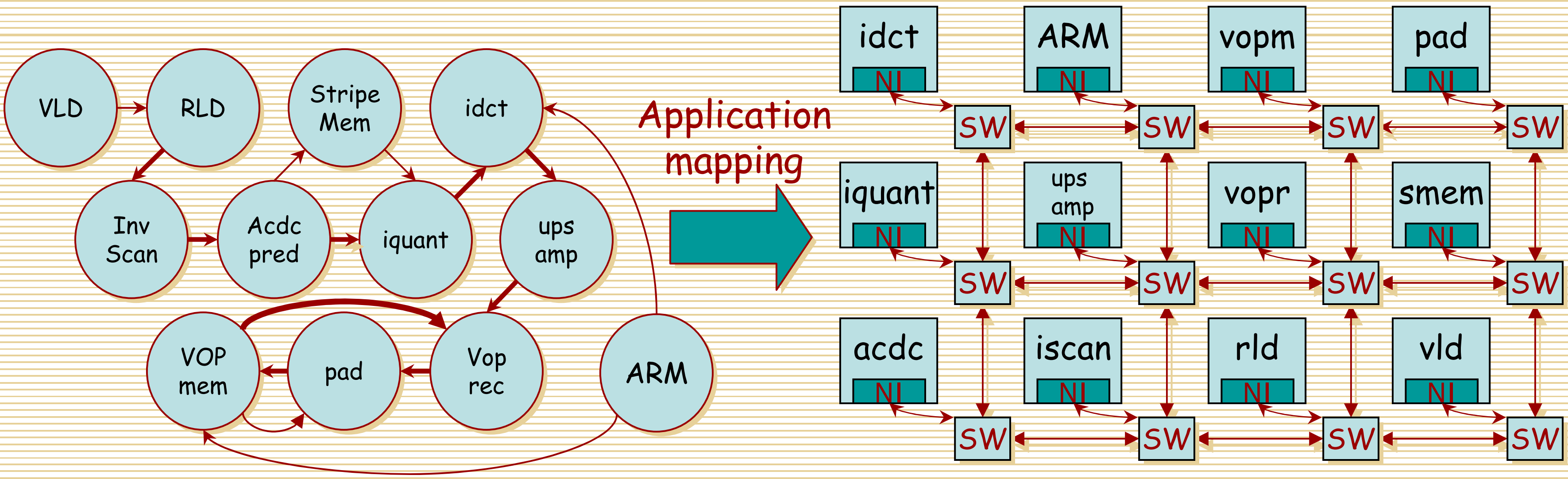


- ACK/nACK Flow & Error Control
- 2-stage pipelined
- High Speed (1GHz @ 130nm)
- Wormhole Switching
- Arbitration: Fixed / RR
- Source Based Routing

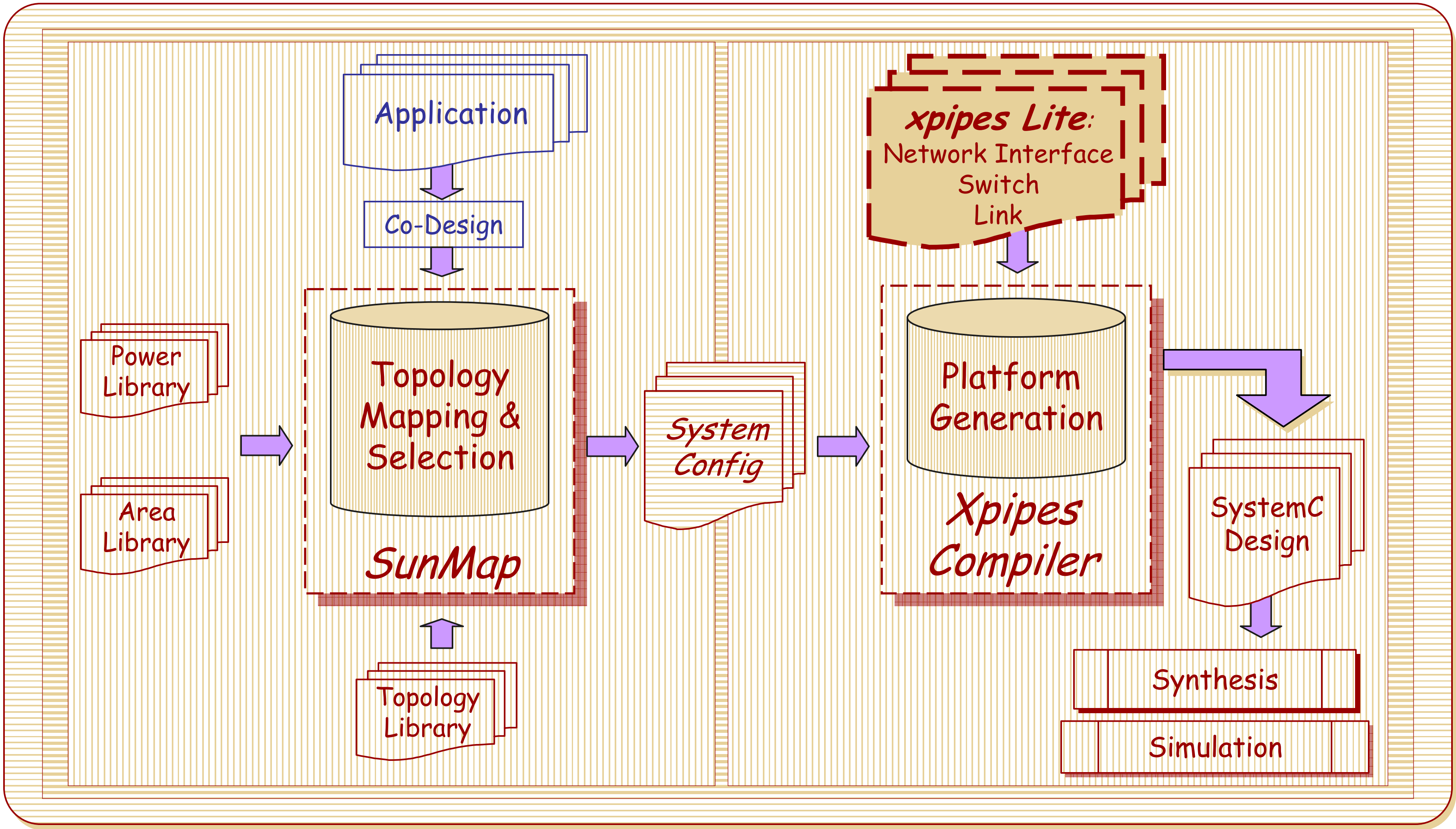
High Level View

- Typical SoC Application Characteristics
  - Complex
  - Highly Heterogeneous
  - Communication Intensive
- xpipes: Synthesizable, High Performance, Heterogeneous NoC Infrastructure

Example



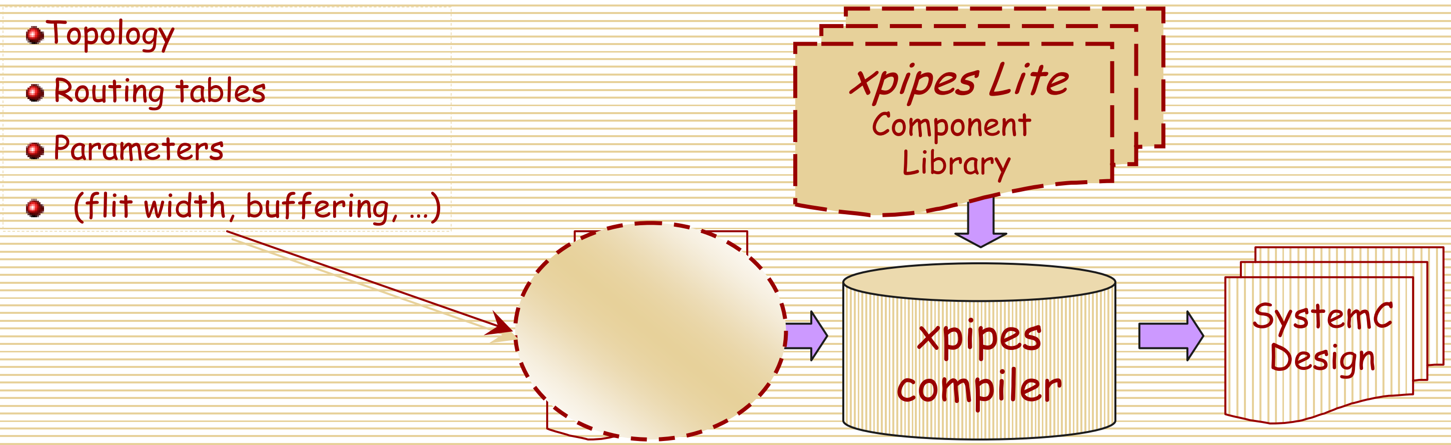
NetChip NoC Synthesis Flow



Topology Instantiation

xpipes Compiler

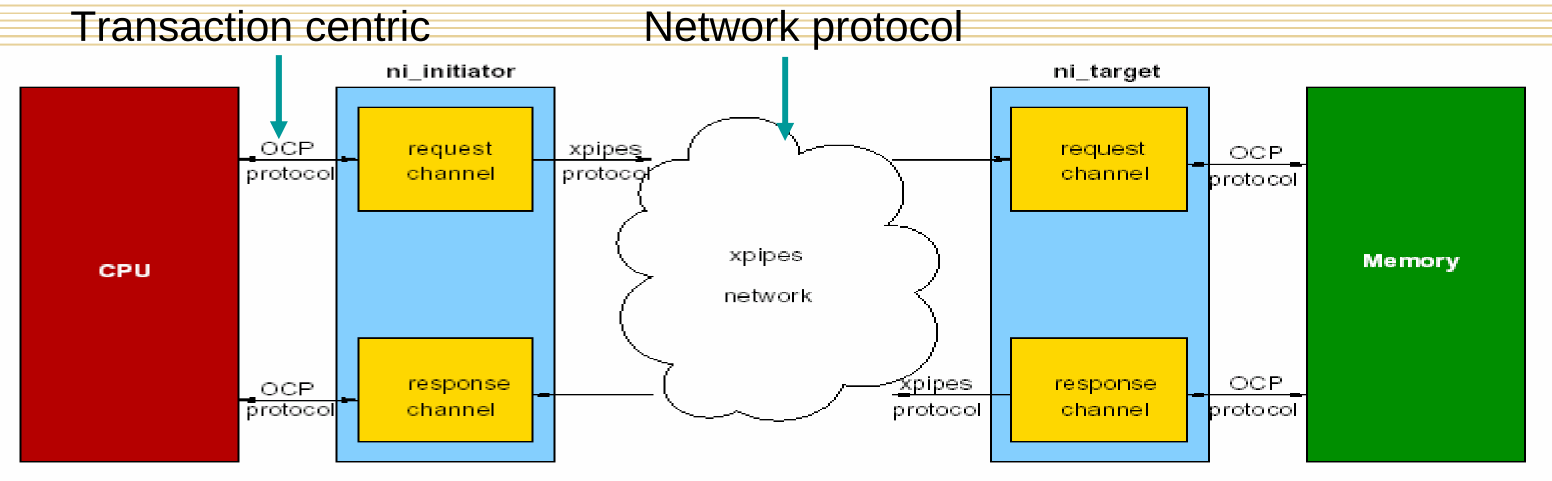
- Creates a Class Template For Each Network Component Type
- Component Optimizations
  - I/O Ports
  - Buffer Sizes
- Hierarchical System Instantiation
  - Synthesis View
  - Simulation View



- Topology
- Routing tables
- Parameters
- (flit width, buffering, …)

Xpipes Lite: Network Interface

Network Interface

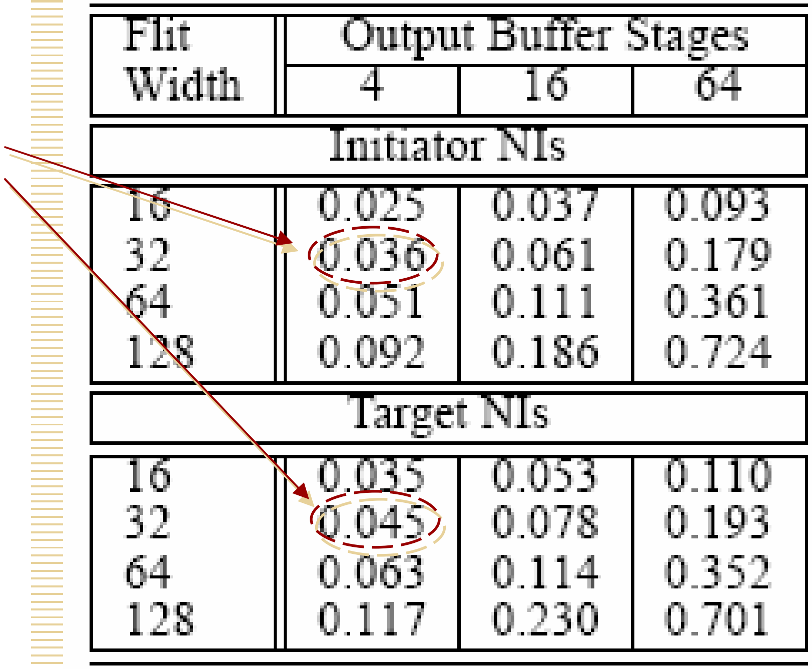


Transaction centric

Network protocol

NI Synthesis Results

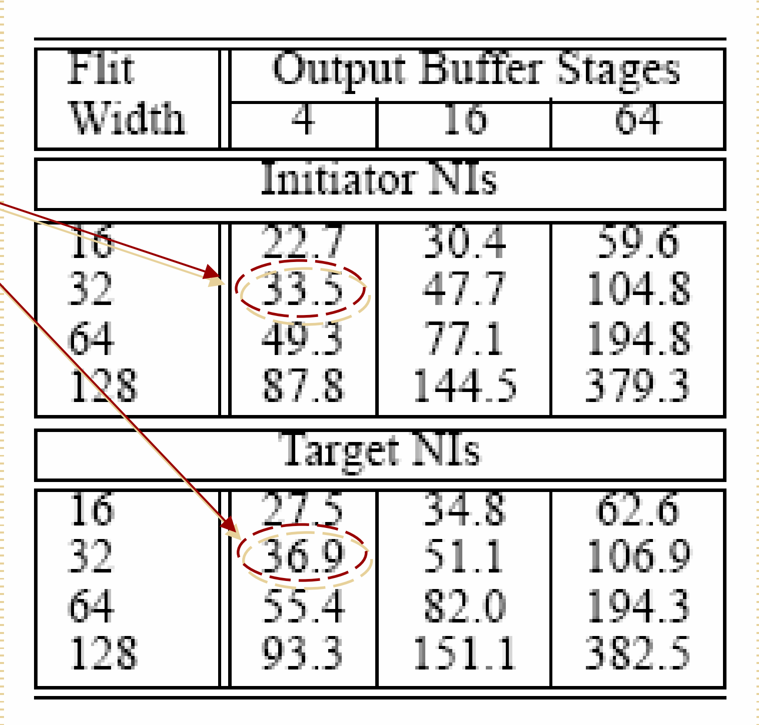
Area (*mm^2*)



Flit Width	Output Buffer Stages		
	4	16	64
Initiator NIs			
16	0.025	0.037	0.093
32	0.036	0.061	0.179
64	0.051	0.111	0.361
128	0.092	0.186	0.724
Target NIs			
16	0.035	0.053	0.110
32	0.045	0.078	0.193
64	0.063	0.114	0.352
128	0.117	0.230	0.701

NI Synthesis Results

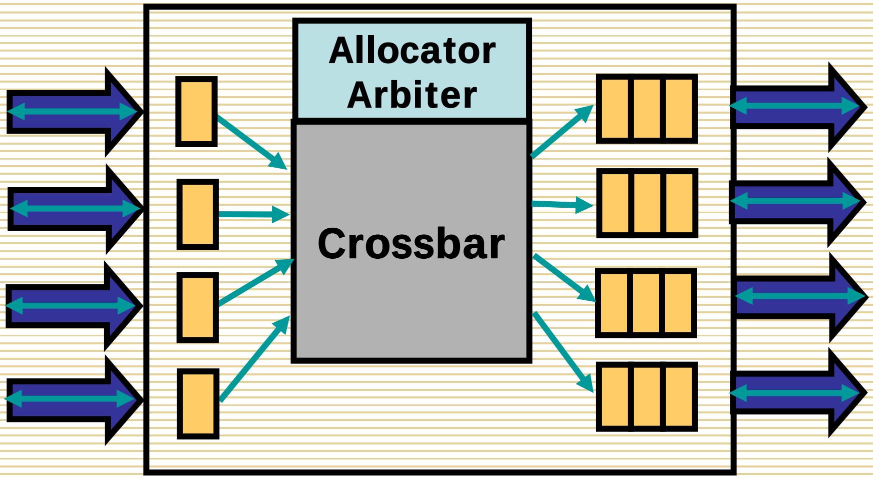
Power (*mW*)



Flit Width	Output Buffer Stages		
	4	16	64
Initiator NIs			
16	22.7	30.4	59.6
32	33.5	47.7	104.8
64	49.3	77.1	194.8
128	87.8	144.5	379.3
Target NIs			
16	27.5	34.8	62.6
32	36.9	51.1	106.9
64	55.4	82.0	194.3
128	93.3	151.1	382.5

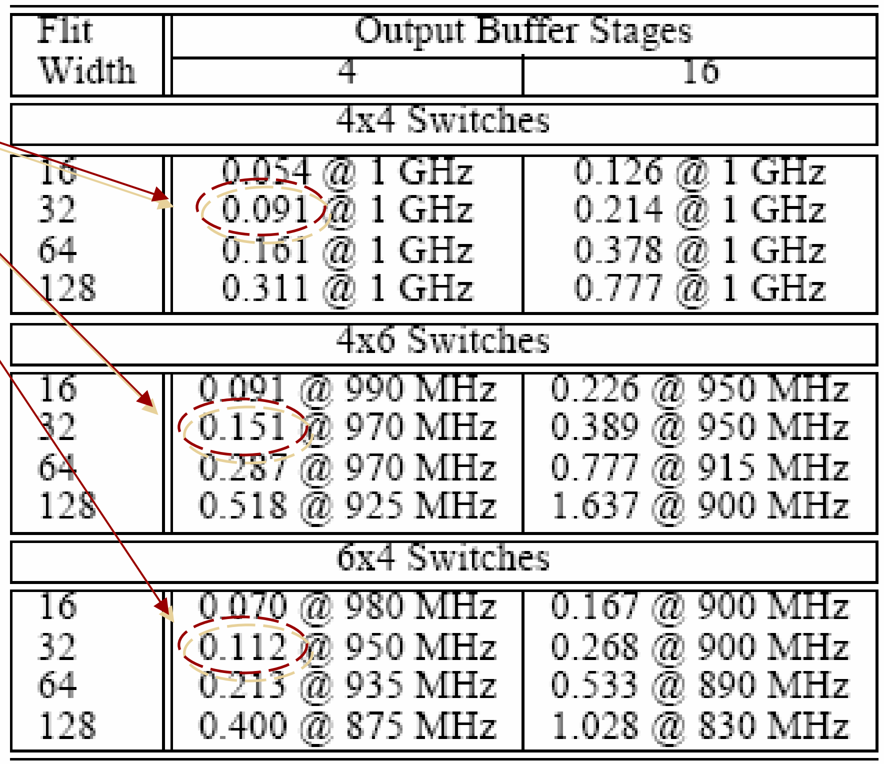
Xpipes Lite: Switch

Switch



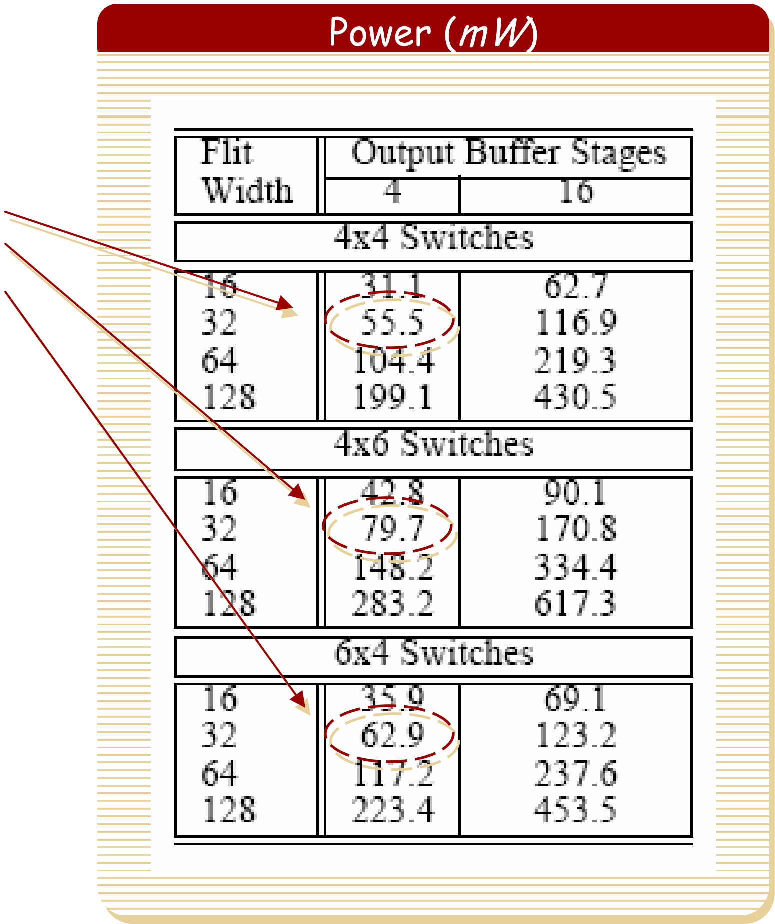
Switch Synthesis Results

Area (mm^2)



Flit Width	Output Buffer Stages	
	4	16
4x4 Switches		
16	0.054 @ 1 GHz	0.126 @ 1 GHz
32	0.091 @ 1 GHz	0.214 @ 1 GHz
64	0.161 @ 1 GHz	0.378 @ 1 GHz
128	0.311 @ 1 GHz	0.777 @ 1 GHz
4x6 Switches		
16	0.091 @ 990 MHz	0.226 @ 950 MHz
32	0.151 @ 970 MHz	0.389 @ 950 MHz
64	0.287 @ 970 MHz	0.777 @ 915 MHz
128	0.518 @ 925 MHz	1.637 @ 900 MHz
6x4 Switches		
16	0.070 @ 980 MHz	0.167 @ 900 MHz
32	0.112 @ 950 MHz	0.268 @ 900 MHz
64	0.213 @ 935 MHz	0.533 @ 890 MHz
128	0.400 @ 875 MHz	1.028 @ 830 MHz

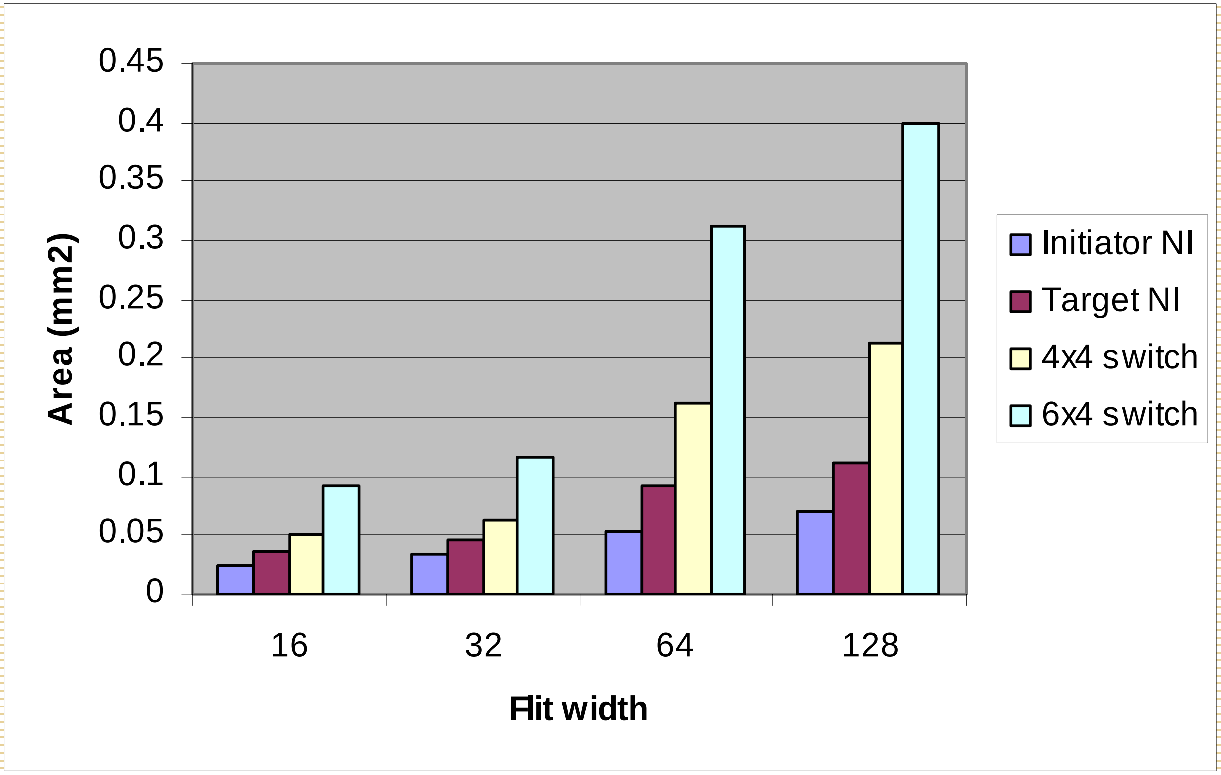
Switch Synthesis Results



Power (*mW*)

Flit Width	Output Buffer Stages	
	4	16
4x4 Switches		
16	31.1	62.7
32	55.5	116.9
64	104.4	219.3
128	199.1	430.5
4x6 Switches		
16	42.8	90.1
32	79.7	170.8
64	148.2	334.4
128	283.2	617.3
6x4 Switches		
16	35.9	69.1
32	62.9	123.2
64	117.2	237.6
128	223.4	453.5

Area Breakdown & Mesh Case Study

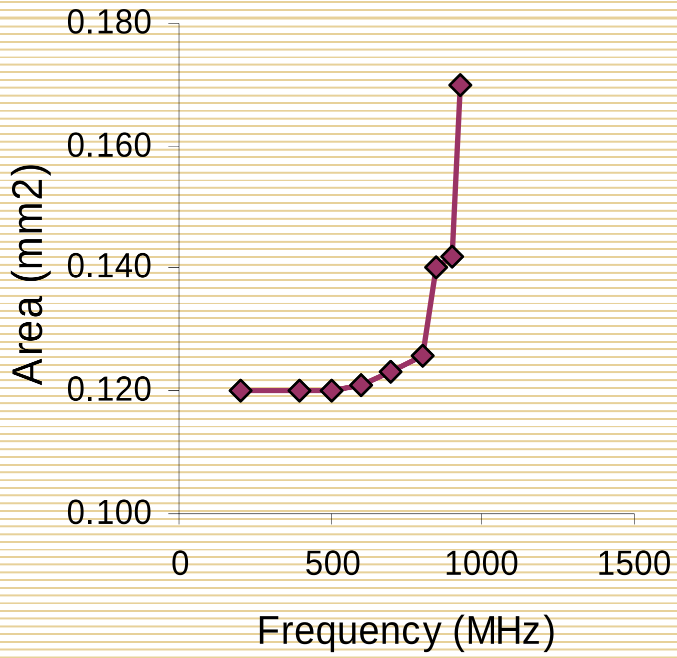


- A 3x4 xpipes mesh for 4 processors and 7 slaves occupies ~2,2 mm^2
- Initiator NI / Target NI / 4x4 Switch @ 1GHZ
- 6x4 Switch @ 875 – 980 MHz

Synthesis Tradeoffs for NoC Soft Cores

- Greater Opportunity for Optimization
- Various Power/Frequency/Area Tradeoffs!

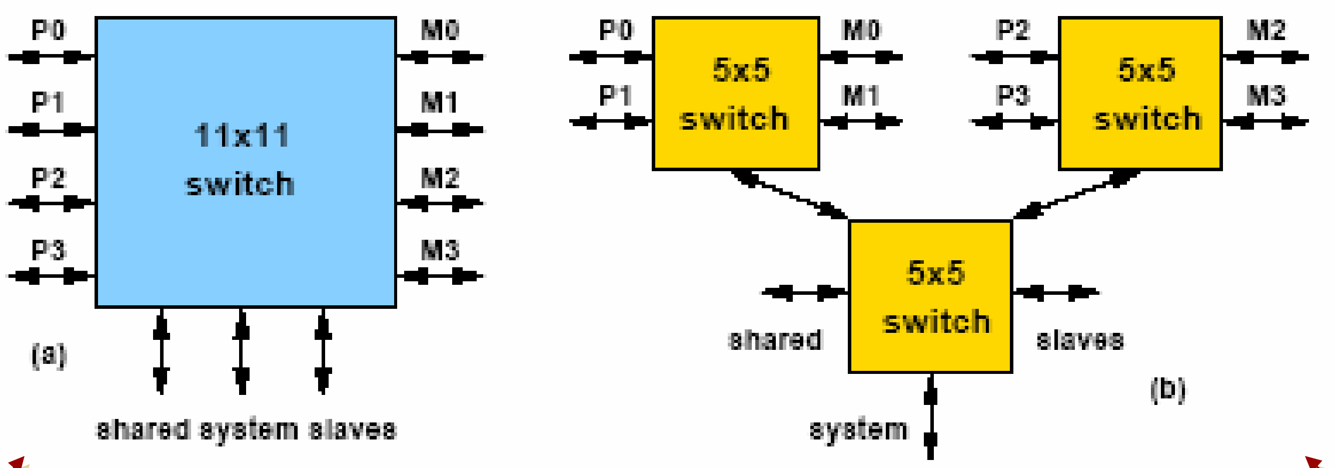
32bit 5x5 Switches



The Power of Abstraction: *Shift Efforts at a Higher Abstraction Layer*

Quick and Accurate Estimations

Sample xpipes Topologies



Fewer Clock Cycles (*Latency Gains*)
However: 780MHZ, .48mm^2 area

925MHZ, .51mm^2 (+10% Performance!)
OR: 850MHz, .42mm^2 (-14% Area)

Conclusion

- Complete Synthesis Oriented Design Flow for NoCs
  - Automatic NoC Generation from Application Graph
  - Parallel Synthesis & Simulation Design Flows
- High Speed, Highly Parameterizable Design Library
  - Allows Faster & More Accurate Design Space Exploration

DEMO

Thank You!

Stergios Stergiou

Stanford University, CA, USA